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DESIGN OF X-BAND POWER AMPLIFIER FOR LEO SATELLITE TRANSMITTER

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ABSTRACT: *The design of a three-stage X-band power amplifier (PA) is presented in this article. The amplifier is realized using an ATF-38143 low noise PHEMT FET. The proposed PA achieves 17–18.3 dB power gain, a good input matching ($S_{11} < -8$ dB) and a good output matching ($S_{22} < -10$ dB). The average power added efficiency when the input power 5 dBm is 50% over the 4-GHz bandwidth (from 8 to 12 GHz). The total power consumption of the PA is 0.24 W from 2.5 V supply voltage. Its performance was simulated using Agilent EEs of ADS simulator. The PA is fabricated with photolithographic technique and scattering parameters are measured using Agilent Vector Network Analyzer ES1978. Measurements and simulations show good agreement.*
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Key words: *low earth orbit; X-band; power amplifiers; PHEMT; inductive degeneration; LPF*

1. INTRODUCTION

Modern satellite communication systems require high data rate, high-efficiency, and simple transmitters, without sacrificing linearity depending on the modulation scheme. Low earth orbit (LEO) satellites dedicated for earth remote sensing applications, especially those concerned with land imaging, use high bit rates for image data downloading to the ground stations. Such satellites usually operate in the X-band of the microwave frequency spectrum. According to the excessive noise at such relatively high frequency and the wideband of operation; it becomes an essential requirement to transmit the data through a high microwave power to the ground stations. Power amplifiers (PA) are among the most important elements in transmission system chains. Optimizing efficiency, linearity, output power, and bandwidth remains a challenging task for the designer although several different design techniques and circuit solutions are available [1]. After PA; LPF is used to eliminate the harmonics generated from the PA and transmitting only the required signal.

The proposed PA is consisted of a three stage common source (CS) amplifier to achieve optimum output power and gain while maintaining a wide bandwidth; the wide bandwidth is achieved by inductive degeneration technique. The proposed PA in this article is simulated using ADS 2009. The PA is fabricated using thin film photolithographic technique. The scattering parameters are measured using vector network analyzer ES1978A. The power measurements are made using spectrum analyzer. The PA is fabricated on Rogers RT5880 substrate with thickness of 1.575 mm, relative permittivity of 2.2 and tan $\delta = 0.0009$.

In Section 2, the PA design concept is illustrated. The proposed PA is presented in Section 3. Measured and simulated results are presented in Section 4. While, the article conclusion is given in Section 5.

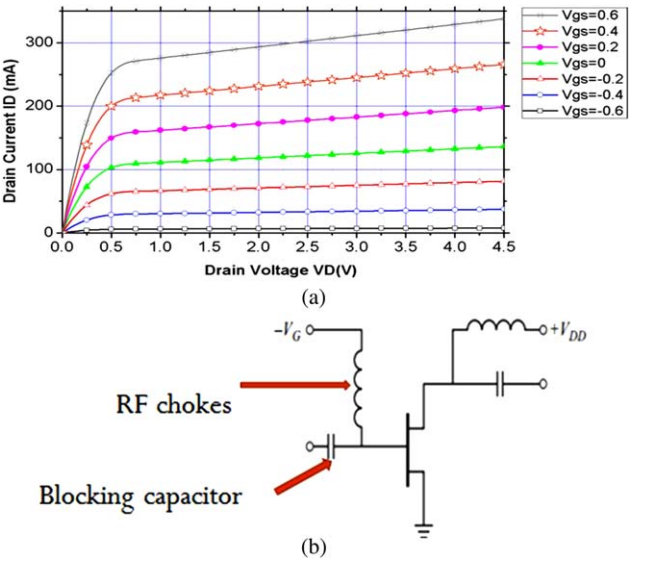


Figure 1 (a) The I-V curve of ATF-38143 and (b) the biasing network used in the proposed PA. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]

2. PA DESIGN CONCEPT

2.1. Transistor Selection

The first step in the design of any amplifier is choosing the suitable transistor. There are two types of transistor bipolar junction transistor (BJT) and FET. BJT is current controlled but FET is voltage controlled. FET amplifiers have greater bandwidth than equivalent BJT topologies. FET amplifier has a smaller voltage gain than BJT. In the proposed PA, design ATF-38143 is used which is high dynamic range, low noise, high IP3, low cost, PHEMT housed in a 4-lead surface mount plastic package and suitable for LEO systems [3].

2.2. Biasing Circuit

After choosing the transistor it is required to estimate the *I-V* characteristic. To estimate the *I-V* curve it is required to build up the circuit shown in Figure 1(a), the gate source voltage is swept from −0.6 V to 0.6 V and the drain source voltage is swept from 0 V to 4.5 V as mentioned in datasheet. The *I-V* curve of ATF-38143 is shown in Figure 1(b). Choosing the suitable Q-point depends on the application (low noise, high gain, high power), the class of the amplifier (class A, class AB, class B), and the transistor. The maximum allowed DC power dissipation of ATF-38143 is equal to 0.58 watts. This value will limit the choice of the bias level to ensure a secure operation region for the transistor.

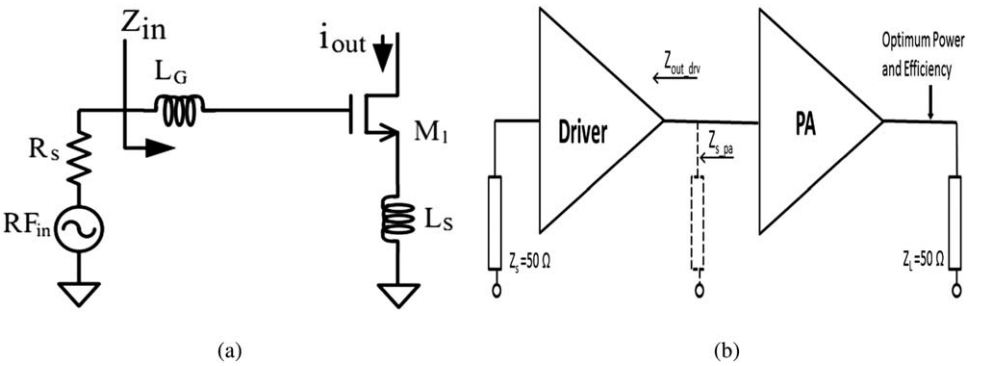


Figure 2 (a) Schematic of the inductive source degeneration technique [5]. (b) The interstage between two stage PA.

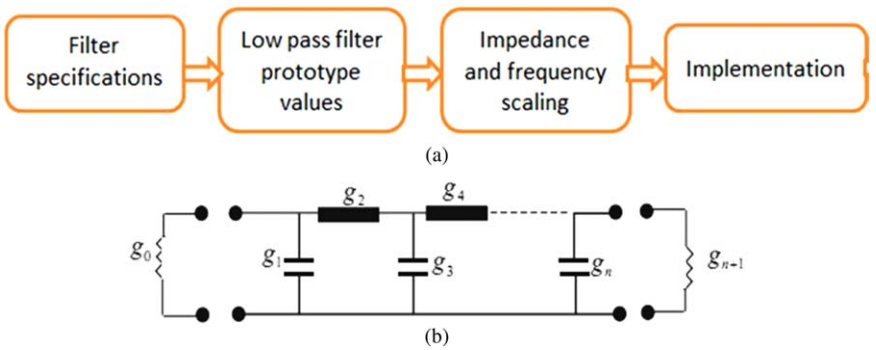


Figure 3 (a) Microstrip filter design steps [8] and (b) odd order Butterworth low-pass prototype filter. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]

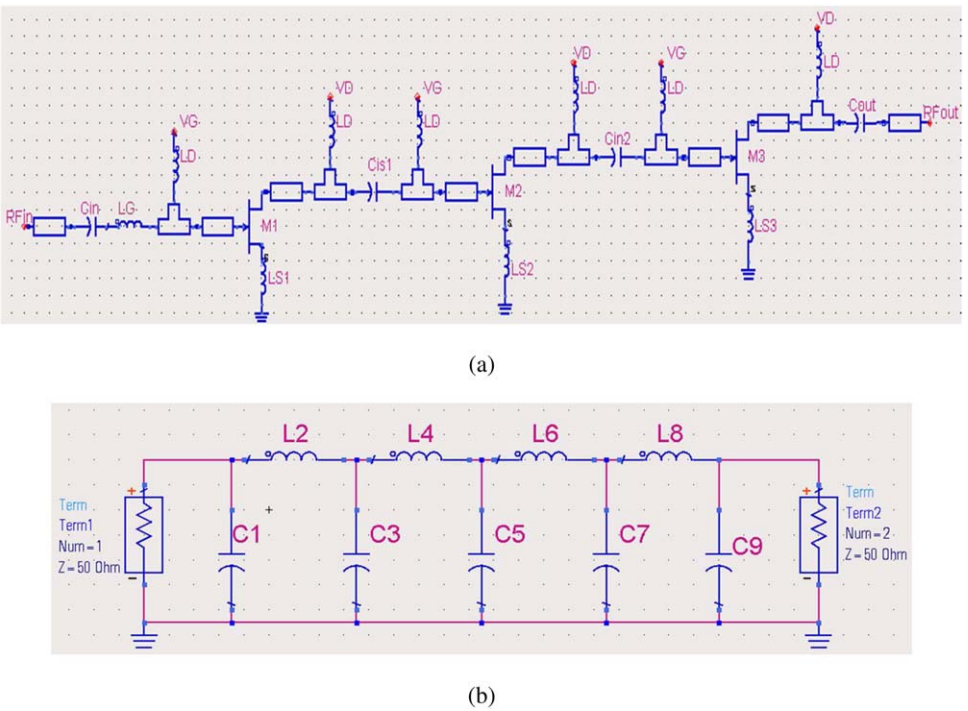


Figure 4 (a) The proposed three stage PA and (b) the proposed nine order Butterworth LPF. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]

TABLE 1 Components for the Proposed PA Shown in Figure 4(a)

Component	L_D	L_G	L_{S1}	L_{S2}	C_{in}	C_{is1}	C_{is2}	C_{out}
Value	55 μH	0.4 nH	0.003 nH	0.125 nH	0.062 pf	0.105 pf	0.052 pf	0.092 pf

TABLE 2 Components for the Proposed LPF Shown in Figure 4(b)

Component	C_1, C_9	L_2, L_8	C_3, C_7	C_5
Value	0.0691 pf	0.49746 nH	0.3048 pf	0.3979 pf

The proposed PA is class B amplifier. The class B amplifier is biased near cutoff region [4]. The proposed PA is biasing with Q-point $V_{GS} = -0.4$ V, $V_{DS} = 2.5$ V, and $I_{DS} = 32$ mA and DC power dissipation is 80 mW for each stage.

2.3. Input Impedance Matching

A traditional impedance matching technique using a source degeneration inductor to achieve acceptable input impedance matching over the desired bandwidth shown in Figure 2 [5, 6]. Our goal is to conjugate match the input port of the circuit to the signal source output impedance RS at a certain resonance frequency ω_o. The bandwidth of this matching technique mainly relies on the quality factor of both the gate inductor L_G and the source inductor L_S. The input impedance of the circuit Z_{in} can be calculated using Eq. (1).

$$Z_{in} = j\left[\omega(L_G + L_S) - \frac{1}{\omega C_{gs}}\right] + \frac{g_{m1} L_S}{C_{gs}} \tag{1}$$

where C_{gs} is the gate-source capacitance and g_{m1} is the transconductance of input device M1. Inductors L_S and L_G are the source degeneration inductor and the gate input inductor. The real part of the input impedance in (1) is given by:

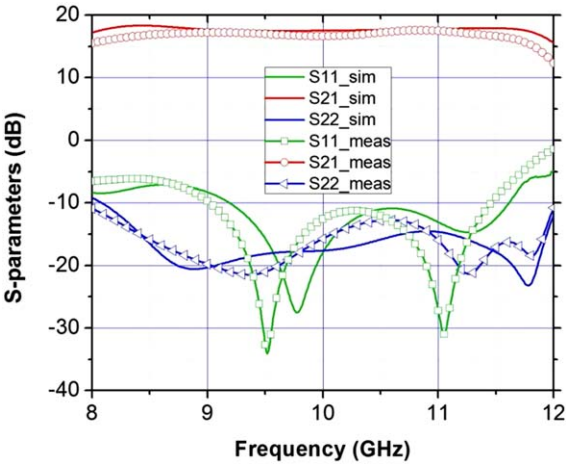


Figure 7 Measured and simulated *S*-parameter of the three-stage PA versus frequency. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]

$$R_S = \frac{g_{m1} L_S}{C_{gs}} = 50\Omega \tag{2}$$

With given values of g_{m1} and C_{gs}, the desired impedance to match to R_S (usually 50Ω) can be obtained by setting L_S accordingly. Next, the imaginary part of the input impedance can be compensated with an input matching inductance L_G. The corresponding resonance frequency is approximated by:

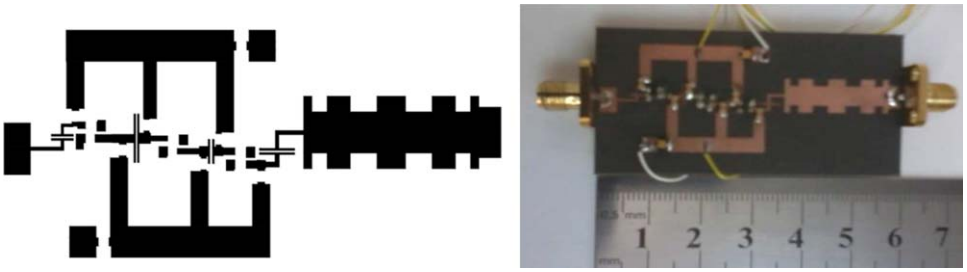


Figure 5 Layout and fabricated PA with LPF. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]

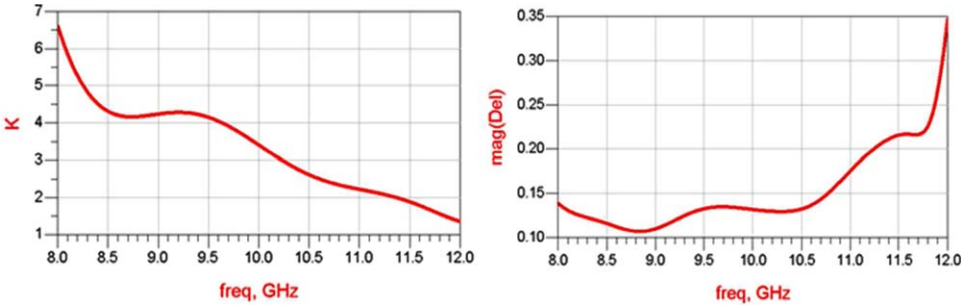
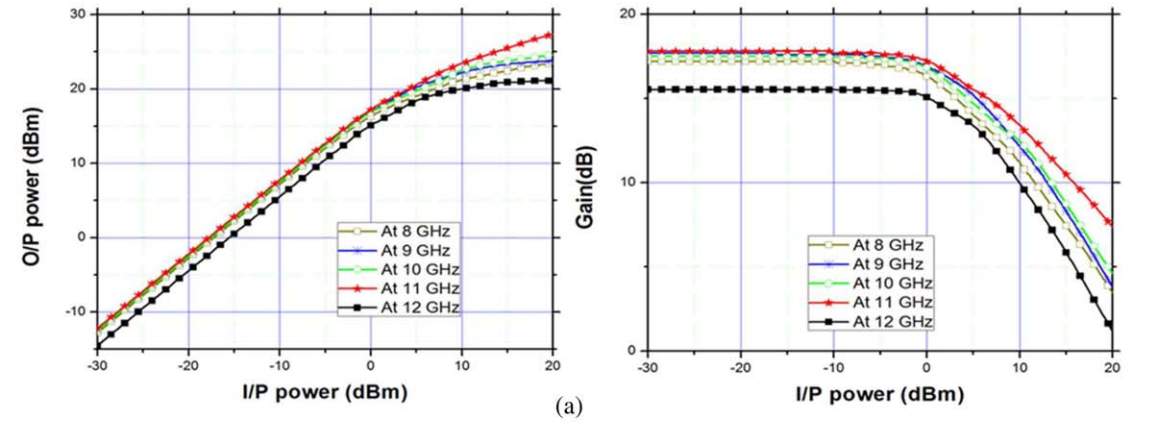


Figure 6 K factor and delta of [*S*] parameters matrix. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]



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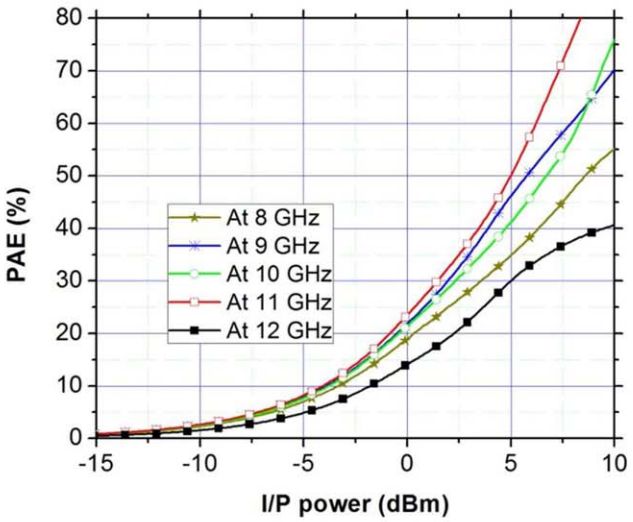

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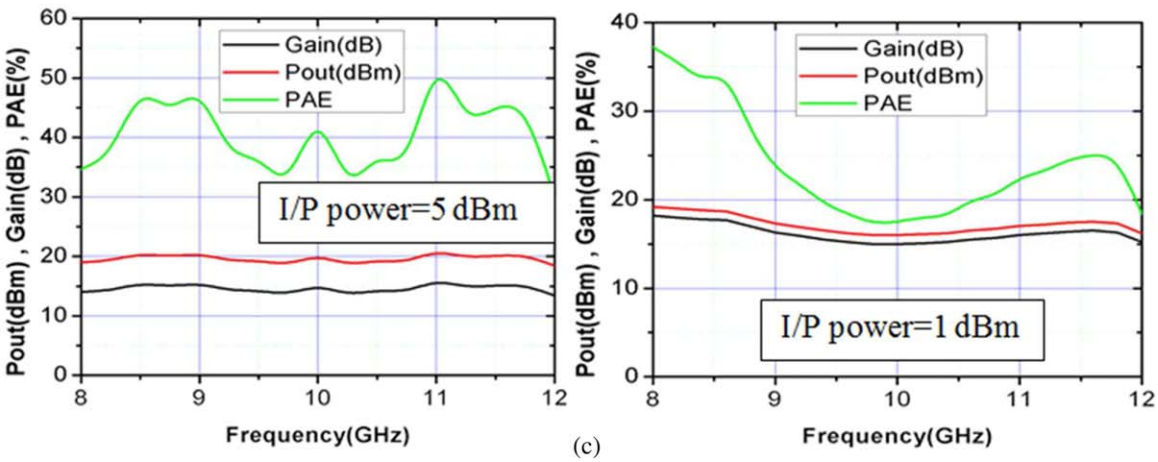


(c)

Figure 8 (a) The simulated output power and gain versus input power and (b) The simulated PAE versus input power. (c) Simulated Pout, Gain and PAE versus frequency. (d) Measured and simulated output power and gain versus input power at 10 GHz. (e) Measured and simulated PAE versus input power at 10 GHz. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]

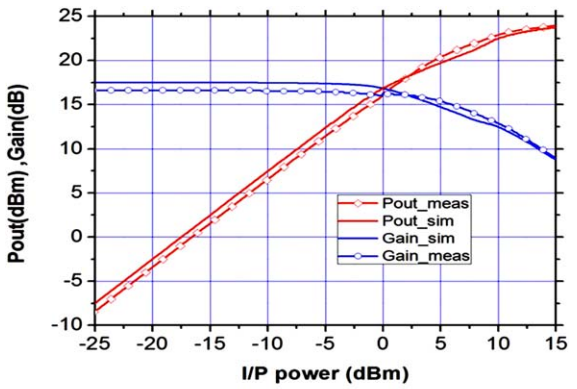
$$\omega_0 = \frac{1}{\sqrt{(L_G + L_S)C_{gs}}} \tag{3}$$

2.4. Interstage Matching

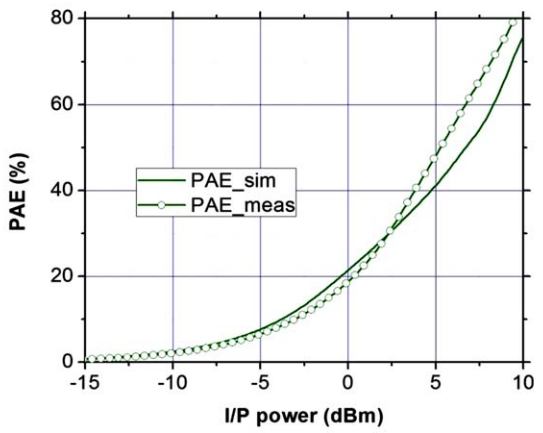
The interstage matching network has been designed to match the optimal load impedance of the driver stage to the conjugate-complex source impedance of the following amplifier stage as shown in Figure 2(b). Passive elements such as capacitors are used for the realization of the matching network in the very same manner [7, 8].

2.5. Low Pass Filter

When the amplifier is operating in the cutoff region, harmonics are introduced in the drain so LPF is adding after PA LPF is used at the output of the PA to eliminate the harmonics



(d)



(e)

Figure 8 Continued

generated by the nonlinearity of the PA. The general filter design steps are shown in Figure 3(a).

First of all, the required filter specifications should be characterized, for example, low-pass, high-pass, or band-pass filter, required cutoff frequency, cutoff rate, and passband characteristics, and so forth. Then choose the required response to be used, maximally flat response or equal ripple, and so forth. The proposed filter is a nine order maximally flat LPF with cutoff frequency of 16 GHz.

The second step is to design the low-pass prototype. For Butterworth response the specific formula to determine prototype values as shown in Figure 3(b) [9, 10]. This formula is

$$g_0 = g_{n+1} = 1 \tag{4}$$

$$g_i = 2\sin\left[\frac{(2i-1)}{2n}\right]; \quad i = 1, 2, \ldots\ldots n \tag{5}$$

The third step in the design process is to shift the prototype response to the required frequency, that is, frequency scaling, then apply impedance scaling for better matching.

Formula to calculate L_i and C_i

$$L_i = \frac{g_i Z_0}{w_c} \tag{6}$$

$$C_i = \frac{g_i}{Z_0 w_c} \tag{7}$$

The fourth step in the design process is to convert all the lumped elements to distributed elements using certain transformations.

3. THE PROPOSED PA

The proposed X-band PA circuit is divided into three stages as shown in Figure 4(a). Each one of three stages is a class B PA. The inductor L_{D1} is used as RF choke to the DC supply. The first stage consists of inductive degeneration CS structure, the source degeneration inductor L_{S1} is added for linearity and stability improvement whereas L_G is needed for the impedance matching between the source impedance and the input of transistor M1. The second and third stages are simple CS structure are added to improve the gain of the PA. Two capacitors C_{is1} and C_{is2} are used as interstage matching networks. DC blockings are provided by capacitors C_{in} and C_{out}.

Finally, a nine order Butterworth LPF is added at the output of PA to eliminate the harmonics generated from the nonlinearity of PA and transmitting only the required signal. The proposed LPF has a cutoff frequency of 16 GHz (frequency of the first harmonic in the X-band PA) Figure 4(b). Show a nine order Butterworth LPF.

The values of all the inductors, and capacitors used in the proposed PA and LPF are listed in Tables 1 and 2.

Then converting the PA lumped elements into distributed elements (spiral inductors and gap capacitors) and the LPF lumped elements (capacitors and inductors) into sections of low and high impedance transmission lines [9]. The whole proposed design are simulated using Agilent Technologies's Advanced Design System (ADS) software. ADS layout and fabricated PA with LPF shown in Figure 5.

4. MEASURED AND SIMULATED RESULTS

4.1. Stability Analysis

Due to a high gain, cascode cell is sensitive to oscillations. That is why linear stability analysis must be performed [11]. Figure 6 shows the *K*-factor and the determinant delta of *S* matrix. *K* exhibits that PA is unconditionally stable between 8 and 12 GHz.

4.2. S-parameters

The *S*-parameters are measured using A Vector Network Analyzer for a drain bias voltage of VD = 2.5 V and a drain current ID = 32 mA. The measurement results, compared to the simulation, are given in Figure 7. This PA achieves a power gain of 17 dB, an input return loss (S_{11}) less than −8 dB, an output return loss (S_{22}) less than −10 dB and a reverse isolation (S_{12}) better than 30 dB over the frequency band of interest (8–12 GHz).

4.3. Power Measurements

The PA was also investigated for its large-signal characteristics. Figure 8(a) shows the simulated output power and gain versus input power at 8, 9, 10, 11, and 12 GHz. Figure 8(b) shows the simulated PAE versus input power. Figure 8(c) shows the simulated performances of the amplifier, (Pout, Gain, and PAE) of the PA in the [8–12 GHz] frequency band when the input power equals 5 and 1 dBm.

Also PA performance was measured using a spectrum analyzer. For the center frequency of 10 GHz, a continues-wave (cw) power measurement was performed for a drain bias of VD = 2.5 V and a drain current of ID = 32 mA. Figure 8(d) shows the measured and simulated output power and gain versus input power at 10 GHz. Figure 8(e) shows the measured and simulated PAE versus input power at 10 GHz. It is cleared from Figure 8(d); the measured power gain amounts to 17 dB, the output 1-dB gain compression of 17.8 dBm (56 mW) and the saturated output power of more than 22 dBm (158 mW) was

measured. When the input power equal to 5 dBm the simulated PAE is 40% and the measured PAE is 48%.

5. CONCLUSION

In this article, a three stage class B X-band PA and LPF are proposed. The average gain of the proposed PA is 17.5 dB and average power added efficiency (PAE) is 40% when input power 5 dBm in the frequency band 8–12GHz. The proposed PA can be used for X-band applications such as LEO satellites. There is a good agreement between simulation results and measured.

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A TUNABLE ULTRAWIDEBAND DIGITAL IMPULSE GENERATOR IN 0.18 μm CMOS

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ABSTRACT: *All digitally reconfigurable ultrawideband (UWB) pulse generator is presented. To achieve independent tuning of the frequency and bandwidth, the variable time delay cell and combining amplifiers for the pulse width control are implemented. In addition, to meet the strict regulation of UWB spectrum mask, the pulse shaper based on weighted summing amplifiers is adopted. The experimental results cover the 3–5.5 GHz, with 500–2000 MHz bandwidth while meeting the −41.3 dBm/MHz power spectral density restriction. The current consumption is only 4 mA at 4 GHz and the chip size is 0.42 mm^2 in 0.18 μm CMOS process.* © 2015 Wiley Periodicals, Inc. Microwave Opt Technol Lett 57:865–868, 2015; View this article online at wileyonlinelibrary.com. DOI 10.1002/mop.28976

Key words: *CMOS impulse generator; ultrawideband; ultrawideband radio frequency integrated circuits (RFIC)*

1. INTRODUCTION

Recently ultrawideband (UWB) systems emerge as an attractive technology for the various applications such as the motion detection radar, and real time location system as well as the low power WPAN applications. Unlike the traditional RF transceivers used for the narrow band communication systems, UWB system transmits very short pulse whose bandwidth is from several hundred MHz up to few GHz. The FCC regulation limits the allowed band of 3.1–10.6 GHz with a power spectral density (PSD) of less than −41.3 dBm/MHz. Moreover, there are very stringent regulations that require the lower PSD, −75.3 dBm/MHz, due to GPS bands. This means that the UWB transmitter demands the strict pulse shaping technique for the spectrum emission restriction. According to IEEE 802.15.4a standard, UWB system for low power data communication uses three channels spaced by about 500 MHz in 3–5 GHz band occupying 528 MHz bandwidth for each channel for the channel collision avoidance. Besides, other UWB applications such as UWB radar, very short pulse width of lower than 1 ns is required for the high detection resolution. Considering the avoidance of 5–6 GHz WiFi zone, up to 2 GHz bandwidth (in other word, 0.5 ns pulse width) is strongly desired. To develop the UWB transmitter satisfying the various needs of the different UWB applications such as the low power WPAN, the high accuracy UWB Radar, and even the location-based systems, the bandwidth and the center frequency of UWB pulse should be independently reconfigurable while consuming low power and being integrated in the CMOS technology. Furthermore, the band shaping is also required to be compliant with the mandatory PSD regulation.

There have been reported a lot of UWB pulse generators [1–6]. These papers are categorized into the fully digital pulse generator type [1–4] and the oscillator (LC, Ring, and Relaxation oscillator) based one [5, 6]. An advantage of digital pulse generator is power efficient scheme because it only dissipates power when the pulse is generated. In addition, the pulse width is usually defined by delay elements that can be tunable. However, it may have the limited sidelobe rejection and require extra filtering to meet FCC regulation.

In this article, a tunable 3–5 GHz fully digital CMOS UWB pulse generator with the independently tunable bandwidth and center frequency is presented. Moreover, the pulse shaping topology enables the filtering and shaping of the digitally generated impulse to meet the PSD requirement without the external off-chip filter component. This also leads us to achieve the low cost and small volume UWB transmitter module. The proposed fully digital pulse generator can reconfigure the center frequency and bandwidth by handling the time delay cell and changing the number of "turned on" combining amplifiers, respectively. Also, to meet the regulation of spectrum mask the pulse shaping is